Delay 25 an ASIC for timing adjustment in LHC

H. Furtado, J. Schrader, A. Marchioro and P. Moreira

CERN-EP/MIC, Geneva Switzerland

Abstract

A five channel programmable delay line ASIC was designed featuring 4 channels that allow to phase delay periodic or non-periodic digital signals and a master channel that can be used to phase delay a clock signal. The master channel serves as a calibration reference guaranteeing independence from process, supply voltage and temperature variations. The phase of each channel can be independently programmed with a resolution of 0.5 ns through an I2C interface. The reference clock frequency can be 32, 40, 64 or 80 MHz. The ASIC is manufactured in a 0.25 µm CMOS technology using radiation tolerant techniques. The measured output jitter for the master channel is 19 ps (RMS) and 24 ps (RMS) for the replica channels.

I. Introduction

Timing distribution is critical in High Energy Physics (HEP) Experiments. The construction of the detectors, different length in cables or even differences in time of flight of particles can lead to timing misalignments in the distribution of signals [1]. It is necessary to guarantee that it is possible to realign these signals and this can be achieved with the programmable delay ASIC proposed here.

The delay25 is an improved version of a previous ASIC [2] used for timing adjustments.

The ASIC can delay digital signals, periodical or non periodical, with a resolution of 0.5 ns up to 32 ns.

It consists of a master delay line which is part of a Delay Locked Loop (DLL), responsible for guaranteeing timing independency from fluctuations on the supply voltage, temperature of operation and fabrication process tolerances. It has four replica channels, that can delay periodical or non-periodical signals, in which the timing is guaranteed by using the control voltage of the DLL.

Because it will be used on systems that sit inside the experiments and therefore subject to high doses of radiation, the ASIC was designed using radiation tolerant techniques [3].

II. Chip Architecture

Fig. 1 shows an overview of the ASIC's architecture. It consists of a master delay line, four replica lines and an I2C interface. The master line is part of a Delay Locked Loop (DLL) which is used to guarantee correct timing on the chip. The DLL, must have a periodic signal at its input. It locks on this signal, using it as a calibration reference. It can work with four different reference frequencies (modes), 32, 40, 64 and 80 MHz. The replica lines can delay periodic or non-periodic digital signals. The I2C interface is used to program the output delay on each line, to enable or disable the outputs, to configure the mode of operation and to reset the DLL.

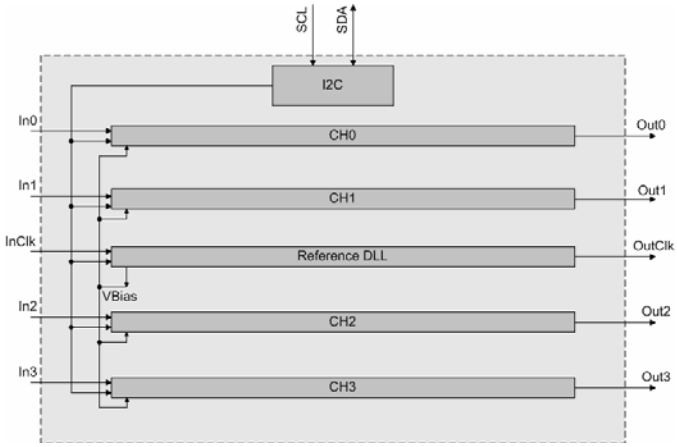

Figure 1 - Delay25 architecture overview

Each one of the five lines consists of 64 Delay Elements (DE). Each delay element is a voltage controlled current starved inverter [4] that, under lock conditions, should have a 0.5 ns delay. Depending on the control voltage, the delay of each element can be as low as half this nominal value and as high as twice as much to be able to cope with process, temperature and power supply variations.

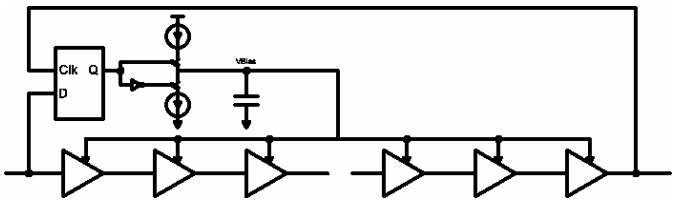

Figure 2 - DLL architecture

Fig. 2 shows a schematic of the DLL. The DLL consists of a line of DEs, a phase detector, a charge pump and a loop capacitor [5]. The signal at the end of the delay line, is compared with the reference signal at its input by the phase detector. The phase detector is implemented as a balanced flip-flop [6] that controls the charge pump which will charge or discharge the loop capacitor, thus speeding up or slowing down the whole line that is, making the delay at each element smaller or bigger. If a rising edge at the end of the line comes first than a rising edge on the reference signal, this means the line is too fast and the filter will tell the charge pump to discharge the capacitor. If on the contrary, the rising edge on the end of the line comes after the rising edge of the reference

signal, the filter will tell the charge pump to charge the capacitor, thus making the line faster. The line will come to a locked state when the total delay on the line is exactly one clock period. The delay at each element is then a function of the period of the input reference signal and of the number of elements in the line and it is equal to T / N (period / number of DEs). Since there are four different input reference frequencies (different clock periods) for each element to have 0.5 ns delay in all modes, the total number of DEs that are part of the control loop must change according to the input frequency. In the 40 MHz (25 ns) case, 50 DEs are necessary to have one clock period delay. If the reference clock is 32 MHz (32 ns) then 64 DEs are necessary. This is achieved by using a multiplexer that chooses how many elements are actually participating in the control loop, as shown in fig. 3.

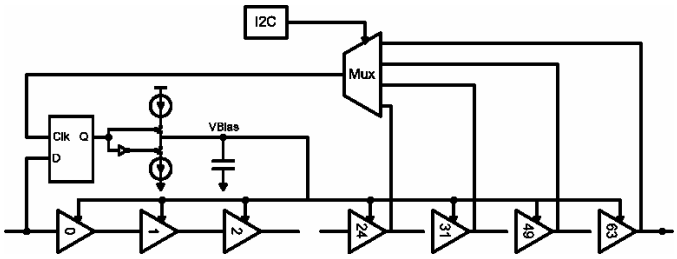

Figure 3 - Different Reference Signal Frequencies

To obtain the user delayed signal, the output form every DE is connected to a multiplexer, like is shown on fig. 4.

The I2C interface is used to select which input of the multiplexer will be present at its output. Thus the number of DEs between the input and the output of a certain channel is chosen, making possible to control the delay in intervals of 0.5 ns.

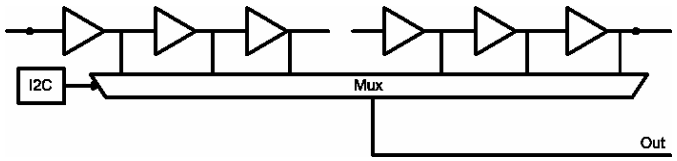

Figure 4 - Getting the delayed signal

The bias voltage generated by the DLL for self calibration is used to control the delay of the replica line DEs. If it is guaranteed that the DEs of the replica lines are exact physical replicas of the ones in the master line (due to good matching) then, this same voltage will make the DEs in the replica lines have the same delay, that is, 0.5 ns each.

The I2C interface is used to program the delay value individually for each channel, enable or disable its output, to configure the operation mode and to reset the DLL.

III. Measurements

Several different measurements were performed on the ASIC and are shown here. All the measurements shown were made with a reference clock of 40MHz and at room temperature.

Fig. 5 shows the measured delay vs. programmed delay for the CMOS mode (similar results are, of couse, obtained in the LVDS mode). The result is close to a straight line thus demonstrating the correct behavior of the circuit.

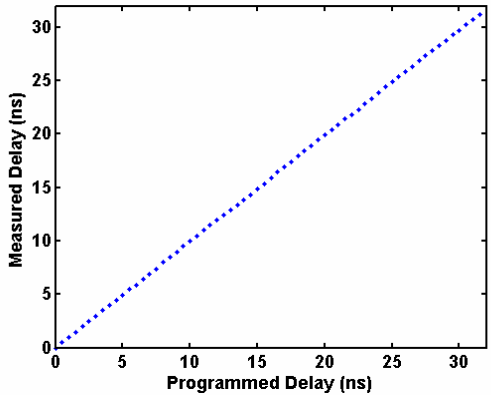

Figure 5 - Circuit Functionality (CMOS)

The integral and differential non-linearity (INL and DNL), were measured, both in the CMOS and LVDS modes, for the DLL channel and one of the replica channels. Both INL and DNL are below 10% of the nominal delay of one element.

As can be seen if fig. 6, the difference between CMOS and LVDS modes, is not of significance for both the INL and the DNL. In the DNL plots three points can be seen where the error is higher than average.

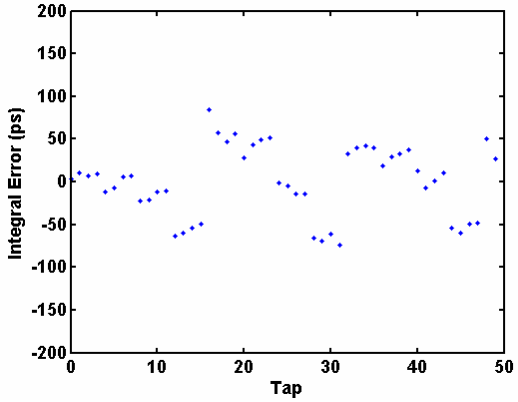

Figure 6a - Integral non-linearity (CMOS)

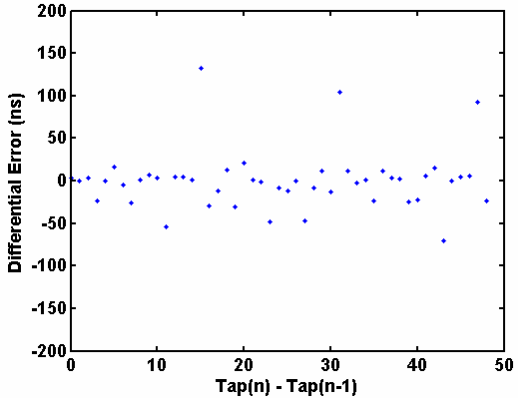

Figure 6b - Differential non-linearity (CMOS)

These points appear systematically and they are related to the topology of the multiplexer indicating that this block has a significant contribution for the total error.

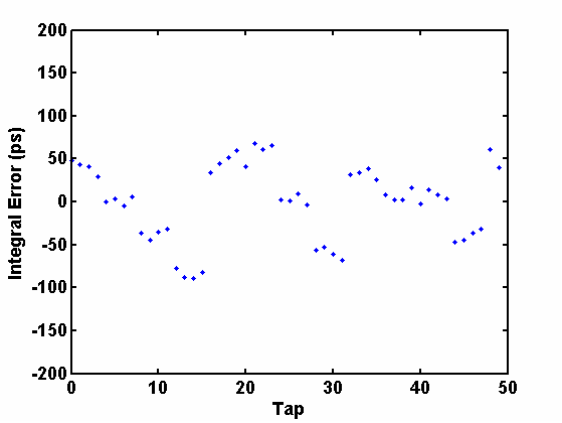

Figure 6c – Integral non-linearity (LVDS)

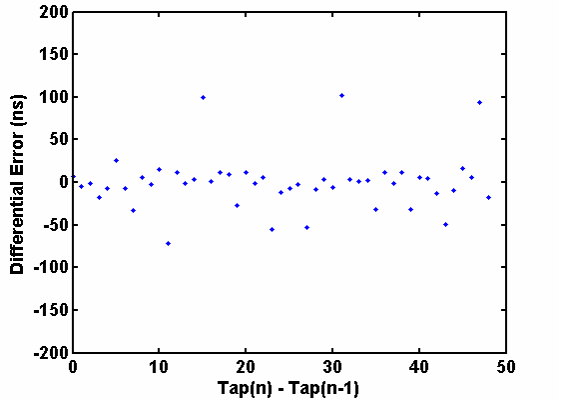

Figure 6d - Differential non-linearity (LVDS)

As for the replica channels all the measurements shown in fig. 7 reveal that the INL is slightly higher than in the master line but this is not true for the DNL. This reveals good matching between the delay elements along each line.

The measured slopes of the delays curves are 497.5 ps/delay-element for the master delay line and 494.7 ps/delay-element for the replica delay lines. This also reveals a global good matching (0.3% error for the master line and 0.9% for the replica lines) between the master and the replica delay lines.

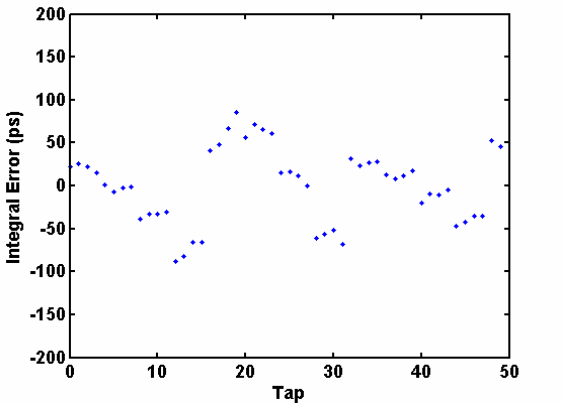

Figure 7a - INL for one replica channel

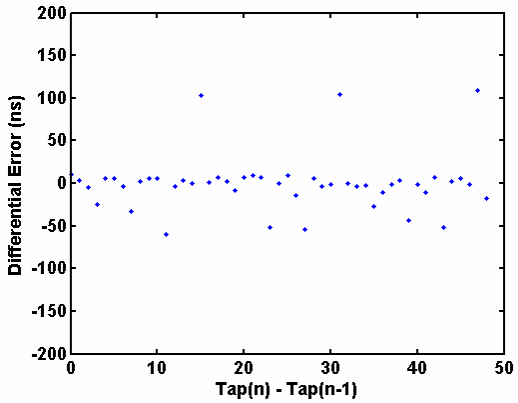

Figure 7b - DNL for one replica channel

Fig . 8 shows measurements made on a replica channel with a 25 ns pulse as input signal. The pulse width at the output was measured to be able to evaluate the pulse distortion of the line. The distortion increases along the line and the maximum value is of 0.5 % of the pulse width, resulting on almost no distortion of the input pulse for maximum delay.

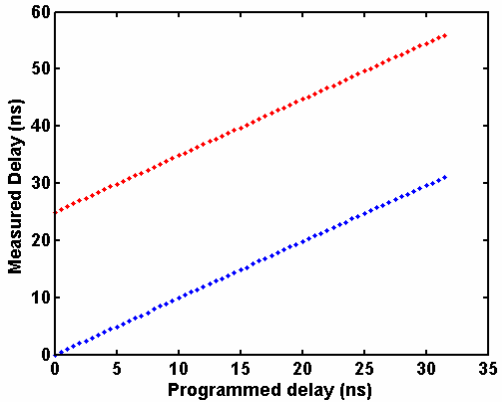

Figure 8a - Pulse rising and falling edge delay

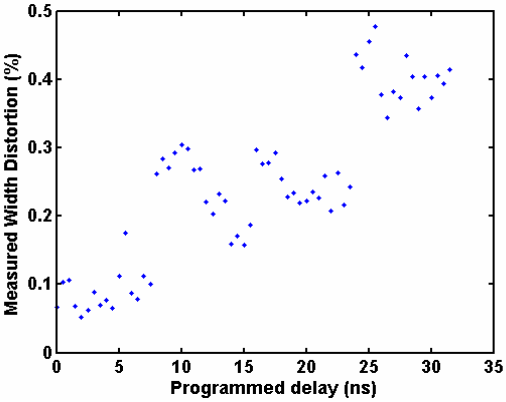

Figure 8b - Pulse width distortion

Fig 9 shows a plot of jitter along the line for the master channel and for one of the replica channels. The measurement shown was made in the LVDS mode. The results in CMOS mode are similar as they were for the INL and the DNL.

In the master channel case, it is seen that the jitter is 15 ps (RMS) at TAP 50 (the last DE participating in the control

loop) and is 19 ps (RMS) at the end of the line. For the replica channel, where there is no control, the jitter is 18 ps (RMS) at TAP 50 and 24 ps (RMS) at the end of the line.

The graphs clearly show that the jitter increases along the delay lines, as expected. The jitter observed at the last tap participating in the control loop is essentially due to the action of the DLL.

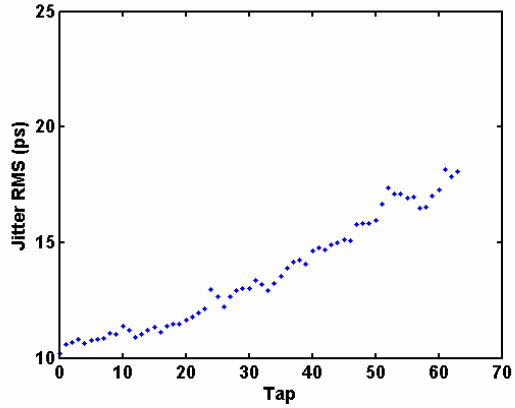

Figure 9a – RMS Jitter along the line (CLK)

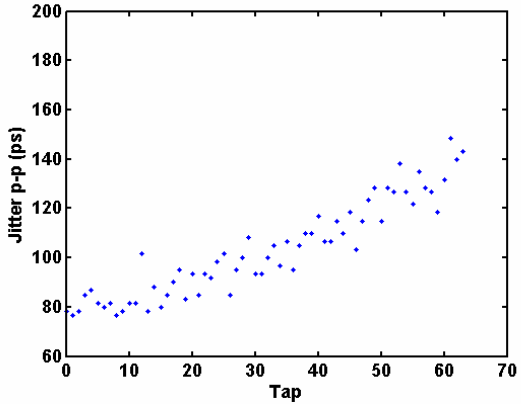

Figure 9b – Peak-to-Peak Jitter along the line (CLK)

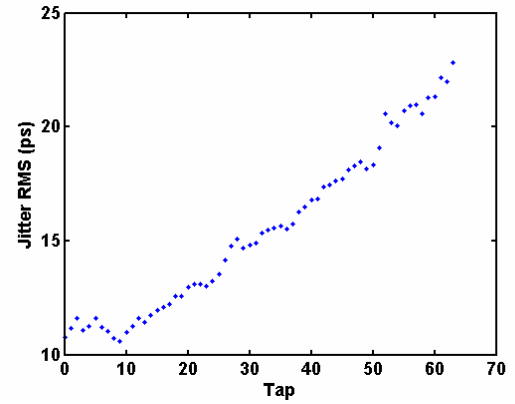

Figure 9c - RMS Jitter along the line (CH0)

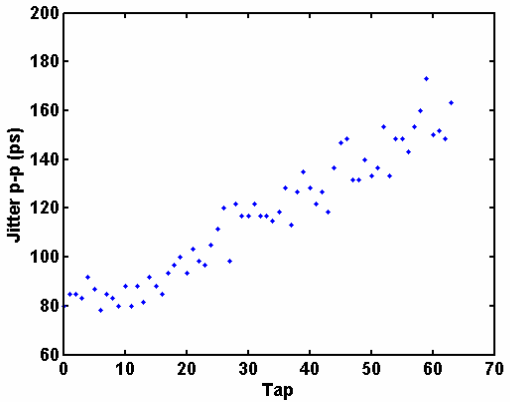

Figure 9d - Peak-to-Peak Jitter along the line (CH0)

On fig. 10 the influence of crosstalk on the measured jitter in one of the replica channels can be seen. The measurement is the same the one in fig. 9c and 9d, but this time with a periodic signal going through one of the other replica channels. The disturbing signal had the same frequency and was in phase with the measured signal. Basically no influence is detected being the jitter values practically the same as in the case without crosstalk.

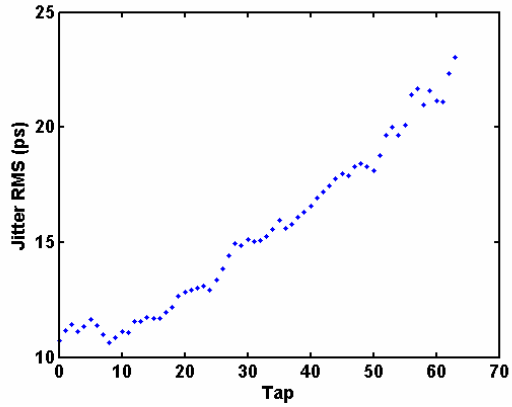

Figure 10a – RMS Jitter with crosstalk (CH0)

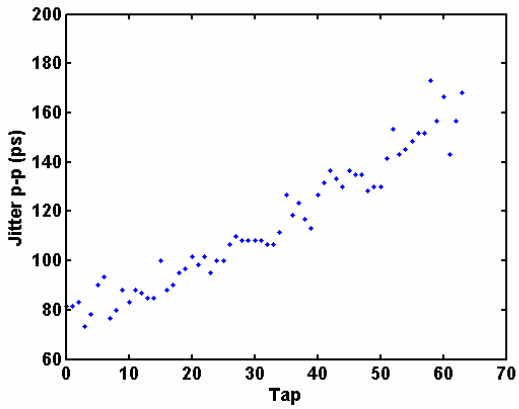

Figure 10b – Peak-to-Peak Jitter with crosstalk (CH0)

The same measurement was made with an asynchronous disturbing signal and the results obtained were similar. This indicates negligible crosstalk between the delay lines in what concerns jitter performance.

Next, fig 11 shows the influence of crosstalk on INL and DNL. There is an increase of 2 ps in both values, in the case where an uncorrelated signal was used as the disturbing signal. No influence has been seen for the correlated case, In any case, the values are still below 10% of the delay of one element.

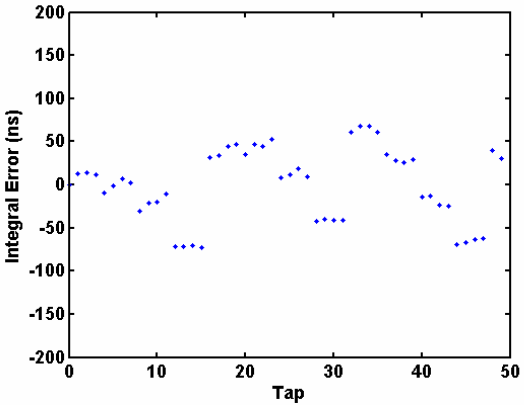

Figure 11a - Influence of crosstalk in the INL

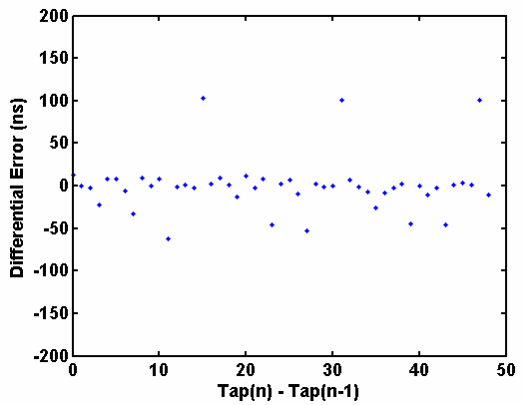

Figure 11b - Influence of crosstalk in the DNL

Finally the total power consumption is around 130 mW. In the 40 MHz mode, the locking range is between 25 and 60 MHz and the chip works with a supply voltage between 2.2 and 2.8 V.

IV. Conclusions and Future Work

The Delay25 was designed in a 0.25 µm CMOS technology. It is intended to be used for timing alignment of digital signals in the LHC experiments.

It has been tested regarding functionality, integral and differential errors, jitter and crosstalk between channels.

Its correct functionality was demonstrated. The measured integral non-linearity is 44 ps and the differential non-linearity is 35 ps. They are both below 10% of the delay of one element.

The influence of crosstalk on the behavior of the circuit was evaluated. The influence on output jitter on the INL and DNL was measured. The measurements were made on a replica channel, but with the presence of a disturbing signal on one of the other replica channels. Two disturbing signals were used, both with 40 MHz, one of them in phase with the measured signal (correlated) while the other was uncorrelated. No real influence can be seen on any of the three parameters, except for a very small increase (2 ps) on the INL and DNL for the uncorrelated case.

Further characterization is undergoing to assess the radiation tolerance of the ASIC.

V. References

[1] B.G. Taylor, "Timing Distribution at the LHC", Proc. 8th Workshop on Electronics for LHC Experiments," Colmar, France, 9-13 September 2002, CERN 2002-003, pp. 63-74.

[2] T. Toifl, R. Vari, "A 4-Channels Rad-Hard Delay Generator ASIC with 1ns minimum time step for LHC experiments", Fourth Workshop on Electronics for LHC Experiments.

[3] G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Florian, A. Giraldo, E. Heijne, P. Jarron, K. Kloukinas, A. Marchioro, P. Moreira, and W. Snoeys, "Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: practical design aspects", IEEE Trans. Nuclear Sciences. Vol. 46 No.6, p.1690, 1999.

[4] Christiansen, J., An integrated high-resolution CMOS timing generator based on an array of Delay Locked Loops, IEEE Journal of Solid-State Circuits, Vol.31, No.7, pp. 952-957, Jul. 96.

[5] M. Mota, " Design and Characterization of CMOS High-Resolution Time-to-Digital Converters ", Ph.D. Thesis at the UNIVERSIDADE TÉCNICA DE LISBOA INSTITUTO SUPERIOR TÉCNICO, Portugal, October 2000

[6] Kim, L. et al., Metastability of CMOS latch/flip-flop, IEEE Journal of Solid-State Circuits, Vol. 25, No. 4, pp. 942-951, Aug. 90.