DELAY25: A 4 channels ½ ns programmable delay line

Description:

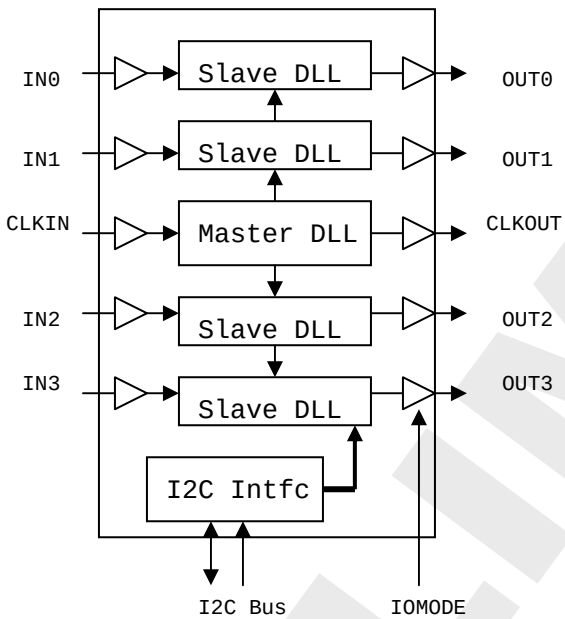
The Delay25 is a 4 channel CMOS programmable delay line. The ASIC is realized in a 0.25 um CMOS radiation tolerant technology. It features a master and four slave Delay Locked Lines: the master is used to lock onto an incoming 40 MHz clock while the four slaves are used to delay four input signals up to 25 ns in steps of ½ ns.

The operation of the chip is controlled through a standard I2C interface.

Features:

- Clock controlled delay line
- Programmable LVDS/CMOS(2.5V)compatible I/O
- 0.5 ns resolution
- Reference clock input: 40/80/32/64 MHz
- Output jitter: < 19 ps (rms)
- Package: TQFP32
- Power supply voltage: 2.5V
- Radiation tolerant
- 0.25 μm CMOS technology

Functional diagram:



Internal I2C register map

I2C Address	Name	Function
0	CR0	Control register channel 0
1	CR1	Control register channel 1
2	CR2	Control register channel 2
3	CR3	Control register channel 3
4	CR4	Control register clock channel
5	GCR	General control reg
6-7	Unused	

Bit allocation in channel CR

B7	B6	B5	B4	B3	B2	B1	B0
n.u	EN OUT	Del5	Del4	Del3	Del2	Del1	Del0

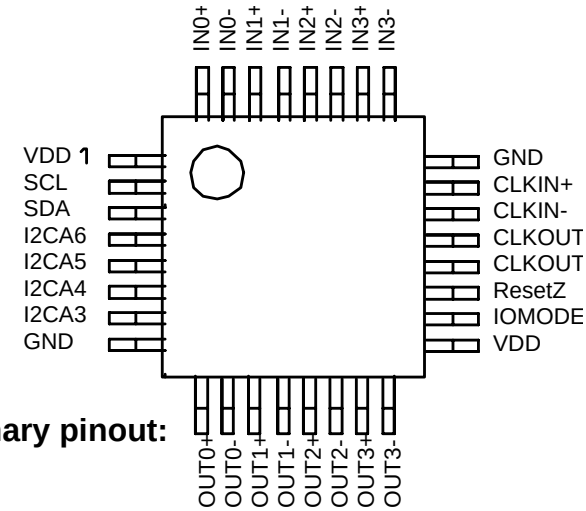
Bit allocation in GCR

B7	B6	B5	B4	B3	B2	B1	B0
reserved	IDLL	n.u.	n.u.	n.u	n.u	M1	M0

Configurable IO mode:

The IN and OUT signals can be configured to comply either to the LVDS standard (IN+/IN- and OUT+/OUT- pairs used) or to a 2.5 V CMOS level mode (IN+ and OUT+ pins). The mode is selected through setting the IOMODE signal to low (0 V) or high (2.5 V) respectively.

Preliminary pinout:



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Modes description:

Clock Mode:

The clock source of the Delay25 ASIC can be selected to be one of the following four:

Mode	Clk Freq
0	40
1	80
2	32
3	64

Modes description:

IO Mode:

The pin IO mode of the Delat25 chip can be configured as follows

IOMode	Function
0	CMOS
1	LVDS

Bit allocation in General Control register:

Bit	Function
1-0	Selects the frequency mode of operation, bits are RW Not cleared by ResetZ
3-2	unused
4	unused
5	unused
6	Init DLL. Writing a 1forces a resync without resetting the chip. Always read as 0.
7	reserved